Fall ’19 CIS 314 Final Review

You may bring two pages of notes, front and back. Questions will be in short-answer format with partial credit for partial answers. Questions will require you to read and write C and Y86-64 code.

Topics:

- All midterm topics, although the exam will focus on material after the midterm
- Y86-64 instructions (all): functionality, operands, byte encoding (general, not specific)
- Y86-64 Register conventions: %rdi, %rsi, %rdx, %rax only
- Circuits: AND, OR, NOT, XOR gates, multiplexers, latches
- Y86-64 processor stages (IF, ID, EX, MEM, WB, PC), signals used in each stage
- Optimizations: code motion, removing procedure calls and memory references, loop unrolling
- Caching: temporal/spatial locality, direct-mapped caches, 2-way set associative caches

Sample questions:

1. [10] Describe the functionality of each Y86-64 processor stage during execution of an addq instruction in terms of the icode, ifun, rA, rB, valC, valP, valA, valB, valE, valM, cnd signals (you may also use M, R, PC, and CC):

IF:

ID:

EX:

MEM:

WB:

PC:

2. [25] Consider a 16B direct-mapped cache with 8B blocks and 2 sets for an 8-bit architecture (i.e., 256 bytes of memory):

a. (5) How many address bits are used to represent the cache set?

b. (5) How many address bits are used to represent the cache tag?

c. (15) Consider the following sequence of memory accesses. For each address, show the tag, set, offset, and whether it resulted in hit or miss:

0x00
0x08
0x04
0x0a
0x00