CIS 314 : Computer Organization

Lecture 1 – Introduction
What is Computer Organization? Where is the HW/SW Interface?

* Coordination of many levels (layers) of abstraction
Levels of Representation

High Level Language Program (e.g., C)

Compiler

Assembly Language Program (e.g., MIPS)

Assembler

Machine Language Program (MIPS)

Machine Interpretation

Hardware Architecture Description (e.g., Verilog Language)

Architecture Implementation

Logic Circuit Description (e.g., Verilog Language)

temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;

lw $t0, 0($2)
lw $t1, 4($2)
sw $t1, 0($2)
sw $t0, 4($2)

wire [31:0] dataBus;
regFile registers (databus);
ALU ALUBlock (inA, inB, databus);

wire w0;
XOR (w0, a, b);
AND (s, w0, a);
Anatomy: 5 components of any Computer

Processor
- Control ("brain")
- Datapath ("brawn")

Memory
(when programs, data live when running)

Devices
- Input
- Output

Keyboard, Mouse
Disk
(when programs, data live when not running)
Display, Printer
AMD Barcelona microprocessor
Intel i7 microprocessor
Intel i7 microprocessor

[Diagram showing the structure of the Intel i7 microprocessor, including cores, memory controller, memory, instruction decode, and execution units.]
Technology Trends: Processor Performance

The graph shows the performance trend of processors from 1978 to 2012. The performance is measured in terms of MIPS (Million Instructions Per Second) and MIPS per Watt. Key milestones include:

- **1978**: AX-11/780, 5 MHz
- **1980**: VAX-11/785, 1.5 MHz
- **1990**: Sun 4/260, 16.7 MHz
- **2000**: VAX 8700, 22 MHz
- **2004**: AMD Athlon, 2.6 GHz
- **2008**: Intel Core 2 Extreme 2 cores, 3.9 GHz

The graph also highlights the performance gap between different processor types, with a 25% per year growth rate in one sector and a 52% per year growth rate in another. The rightmost column labeled 2010 to 2012 indicates a steady increase in performance.
Technology Trends: Clock Rates
Moore’s Law

• **Gordon Moore** - co-founder of Intel observed and predicted a trend:

• Density of data on a chip would double every year

• (Specifically density of transistors on an integrated circuit)

• True for 4 decades. Has slowed a little to double every 18 months. Expected to continue for at least two more decades.

• Implications: increased performance, decreased cost
Computer Technology - Dramatic Change!

• Memory
  – DRAM capacity: 2x / 2 years (since ‘96);
    64x size improvement in last decade (slowing).

• Processor
  – Speed 2x / 1.5 years (since ‘85);
    100X performance in last decade (slowing).

• Disk
  – Capacity: 2x / 1 year (since ‘97);
    250X size in last decade (slowing).
Instruction Set Architectures

• Different CPUs implement different sets of instructions.

• The set of instructions a particular CPU implements is an *Instruction Set Architecture (ISA).*
  
  – Examples: Intel 80x86 (Pentium 4), IBM/Motorola PowerPC (Macintosh), MIPS, Intel IA64, ...
Instruction Set Architectures - History

- **Accumulator ISA**
  - One register in the CPU for arithmetic called the accumulator
    
    ```
    LOAD ACC, X
    ADD ACC, Y
    STORE ACC, Z
    ```

- **Stack ISA**
  - A stack is used for arithmetic
    
    ```
    PUSH X
    PUSH Y
    ADD
    POP Z
    ```
Instruction Set Architectures

• General Purpose Register ISA
• Three types based on where operands for arithmetic operations can come from.
  – Memory-memory
  – Register-memory
  – Register-register (Load/Store)

MIPS has a Load/Store ISA
Instruction Set Architectures

• Early trend was to add more and more instructions to new CPUs to do elaborate operations
  – VAX architecture had an instruction to multiply polynomials!

• RISC philosophy: Reduced Instruction Set Computing
  – Keep the instruction set small and simple, makes it easier to build fast hardware.
  – Let software do complicated operations by composing simpler ones.
RISC Architectures

• Fixed instruction lengths
• Load/store instruction sets
• Limited addressing modes (ways to access variables in memory)
• Limited operations

• Sun SPARC, IBM PowerPC, MIPS
A Few Famous Computer Hardware Designers

John von Neumann, 1903-1957

John Cocker
1985 Eckert-Mauchly Award Recipient

“For contributions to high performance computer architecture through look ahead, parallelism and pipeline utilization, and to reduced instruction set computer architecture through the exploitation of hardware-software tradeoffs and compiler optimization”

RISC and pipelining

John Hennessy, President
Stanford University
RISC Architecture

David Patterson, Prof. UC Berkeley
RISC Architecture
MIPS Architecture

• MIPS – semiconductor company that built one of the first commercial RISC architectures

• We will study the MIPS architecture in some detail in this class (also used in CIS 429 Computer Architecture)

• Why MIPS instead of Intel 80x86?
  – MIPS is simple, elegant. Don’t want to get bogged down in gritty details.
  – MIPS widely used in embedded apps, x86 little used in embedded; mostly PCs.
Growth of x86 ISA