LECTURE 16-b

Memory
Memories in General

- Computers have mostly RAM
- ROM (or equivalent) needed to boot
- ROM is in same class as Programmable Logic Devices (PLDs),
  - Check section B.12 of the book for more details on Field Programmable Device
Properties of Memory

1) Volatile
   - Memory disappears if power goes out
     • Typical computer RAM

2) Nonvolatile
   - ROM
   - Flash memories
   - Magnetic memories like disk, tape

• RAM: Random Access Memory
  - it takes the same amount of time to address/retrieve any particular part
Simple View of RAM

- Of some word size $n$
- Some capacity $2^k$
- $k$ bits of address line
- Has a read line
- Has a write line
1K x 16 memory

- Variety of sizes
  - From 1-bit wide (width)
- Memory size specified in bytes
- This would be 2KB memory
  - 10 address lines and 16 data lines

<table>
<thead>
<tr>
<th>Memory address</th>
<th>Binary</th>
<th>Decimal</th>
<th>Memory contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000000000</td>
<td>0</td>
<td>0</td>
<td>10110101 01011100</td>
</tr>
<tr>
<td>0000000001</td>
<td>1</td>
<td>1</td>
<td>10101011 10001001</td>
</tr>
<tr>
<td>0000000010</td>
<td>2</td>
<td>2</td>
<td>00001101 01000110</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1111111101</td>
<td>1021</td>
<td></td>
<td>10011101 00010101</td>
</tr>
<tr>
<td>1111111110</td>
<td>1022</td>
<td></td>
<td>00001101 00011110</td>
</tr>
<tr>
<td>1111111111</td>
<td>1023</td>
<td></td>
<td>11011110 00100100</td>
</tr>
</tbody>
</table>
Writing

- Sequence of steps
  - Setup address lines
  - Setup data lines
  - Activate write line
Reading

• **Sequence of steps**
  - Setup address lines
  - Activate read line
  - Data available *after specified amt of time*
Chip Select

- Usually a line to *enable* the chip
- Why do you need to select a chip?

### Control Inputs to a Memory Chip

<table>
<thead>
<tr>
<th>Chip select CS</th>
<th>Read/Write R/W</th>
<th>Memory operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>×</td>
<td>None</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Write to selected word</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Read from selected word</td>
</tr>
</tbody>
</table>
Static vs Dynamic RAM

- **SRAM vs DRAM**
- **DRAM stores charge in capacitor**
  - Disappears over short period of time
  - Must be refreshed, i.e. read its content & write it back
- **SRAM easier to use**
  - Faster
  - Smaller sizes
  - But more expensive per bit
Structure of SRAM

- One memory *cell* per bit
- Logic equivalent
Bit Slice

- Cells connected to form 1 bit position
- Word Select gates one latch from address lines
- Note it selects Reads also
- B (and B not) set by R/W, Data In and BitSelect
Bit Slice can Become Module

- Basically bit slice is a X1 memory
16 X 1 RAM

(a) Symbol
Row/Column

- If RAM gets large, there is a large decoder
- Also run into chip layout issues
- Larger memories usually “2D” in a matrix layout
16 X 1 as 4 X 4 Array

- Two decoders
  - Row
  - Column
- Address just broken up
- Not visible from outside
Realistic Sizes

- Imagine 256K memory as 32K X 8
- One column layout would need 15-bit decoder with 32K outputs!
- Can make a square layout with 9-bit row and 6-bit column decoders