Winter ’11 CIS 314 Final Review

You may bring one page of notes, front and back, and the green sheet from your text book.

You may bring a calculator but shouldn’t need one.

Questions will be in short-answer format with partial credit for partial answers.

Questions will require you to read and write assembly code.

Topics:

- All midterm topics, although the exam will focus on material since the midterm
- IEEE-754 binary/hex to/from decimal, floating-point addition
- Boolean logic: AND, OR, NOT gates, truth tables, sum of products
- SR latches, clocked/data latches
- Logic circuits, half/full adders, decoders, multiplexers
- Single-cycle processor: control line values for add, addi, lw, sw, beq (figure 4.17, p. 322)
- Multi-cycle, pipelined processor: 5 stages
- Pipelined processor: hardware (figure 4.33, p. 345), diagrams (figures 4.43, 4.44, p. 357)
- Determining cycle time: single-cycle and multi-cycle processors
- Data hazards: identifying, forwarding from EX or MEM to later EX, load delay slot
- Control hazards: moving branch determination from EX to ID stage, branch delay slot

Sample questions:

1. [25] Consider the following MIPS code:

   add $t0  $t1  $t2
   add $t3  $t4  $t5
   lw  $t6  0($t0)
   add $t7  $t0  $t6

   a. [5] Identify all data dependencies in the above code:

   b. [5] Assuming no forwarding or load delay slot but that registers can be read and written in the same cycle, how many cycles are stalled when executing the above code? Why?

   c. [5] Assuming forwarding (including register read/write in the same cycle) but no load delay slot, how many cycles are stalled when executing the above code? Why?

   d. [5] Assuming forwarding (including register read/write in the same cycle) and a filled load delay slot, how many cycles are stalled when executing the above code? Why?

   e. [5] Which instruction above could you use to fill the load delay slot? Why?
2. [20] Consider the following single-cycle processor diagram:

![Figure 4.17 (p. 322)](image)

a. [10] What are the values of the RegDst, Branch, MemRead, MemtoReg, MemWrite, ALUSrc, and RegWrite, and zero binary control lines for a beq instruction?

b. [10] What decimal register-number values are sent to the Read register 1, Read register 2, and Write register inputs of the register unit for an add $5 \$6 \$7$ instruction?

3. [10] How many control lines are required for a decoder circuit with 1024 outputs?
Figure 4.33 (p. 345)

Figure 4.43 (p. 357)
Program execution order (in instructions)

lw $10, 20($1)
sub $11, $2, $3
add $12, $3, $4
lw $13, 24($1)
add $14, $5, $6

Figure 4.44 (p. 357)