What is computer architecture?

Technology
Programming Languages
History
Measurement & Evaluation
Operating Systems
Applications

The Secret of Architecture Design:
Measurement and Evaluation
- Architecture Design is an iterative process:
  - Searching the space of possible designs
  - At all levels of computer systems

Creativity
Good Ideas
Cost / Performance Analysis
Good Ideas
Mediocre Ideas
Bad Ideas

Computer Architecture Topics
Input/Output and Storage
Memory Hierarchy
VLSI
Disks, WORM, Tape
RAID
DRAM
L2 Cache
L1 Cache

Parallel Computer Arch. Topics
Interconnection Network
Multiprocessors
Distributed Memory Multipro.
Networks and Interconnections

Topic Coverage
- Performance analysis: metrics and benchmarks (Ch. 1)
- Pipelining: basics, hazards, implementation (App. A, Ch. 2)
- ILP: compiler techniques (Ch. 2)
- Branch Prediction (Ch. 2)
- Dynamic Scheduling and HW speculation (A, Ch. 3)
- Caching (App. C, Ch. 5)
- Symmetric Shared Memory Multiprocessors (Ch. 4)
- Distributed Shared Memory Multiprocessors (Ch. 4)
- Other: multicore, Xbox360, your choice! (handouts, guest lectures)
- Not covered: virtual memory, I/O, buses, networks, embedded systems
Prerequisites
CIS 313, 314
• Instruction sets, assembly language, memory addressing
• Pipelining basics ?
• Caching basics ?

CIS 429/529 Course Goals
• Study of the architecture of contemporary desktop computer CPUs and the techniques by which performance is enhanced.
• Study of parallel architectures and innovations/issues that arise because of parallelism.
• Quantitative analysis and evaluation of computer systems. Methods and criteria for evaluating performance and making design trade-offs.
• Research-oriented approach. Learn to think, read, and write critically, scientifically. Learn to problem solve creatively.

Skills honed in this course
• Quantitative problem solving - algebra, probability
• Quantitative analysis - reading, presenting, analyzing data
• Research skills - synthesis, critical analysis, resourcefulness
• Experimental design - simulation experiments on performance
• Presentation skills - writing and speaking
• Group work - problem solving

Course Assignments
• Homeworks (30%)
  extra problems for graduate students
• Exams (40%)
  midterm and final, extra problems for grads
• Programming assignments (25%)
• Class participation (5%)
• Research Paper (required for grads) (20%)
  8-10 pages + in-class short presentation

Credits for transparencies
• Berkeley architecture course websites
• UIUC architecture course websites

Changes in Computer Types 1988 Computer Food Chain
- Mainframe
- Supercomputer
- Microcomputer
- Workstation
- PC
- Massively Parallel Processors

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Today’s Crossroads: Old to New Conventional Wisdom in Comp. Arch

- Old Conventional Wisdom: Power is free, Transistors expensive
  - New Conventional Wisdom: "Power wall" Power expensive, Xbors free
    (Can put more on chip than can afford to turn on)

- Old CW: Sufficiently increasing instruction Level Parallelism via compilers, innovation (Out-of-order, speculation, VLW, ...)
  - New CW: "ILP wall" law of diminishing returns on more HW for ILP

- Old CW: Multiples are slow, Memory access is fast
  - New CW: "Memory wall" Memory slow, multiplices fast

- Old CW: Uniprocessor performance 2X / 1.5 yrs
  - New CW: Power Wall = IGFET Wall = Memory Wall = Brick Wall
    - Uniprocessor performance now 2X / 0.5 yrs
  - Sea change in chip design: multiple "cores" (2X processors per chip ~ 2 years)
    - More simpler processors are more power efficient

Crossroads: Uniprocessor Performance

- VAX: 25%/year 1978 to 1996
- RISC: +86% 1986 to 2002
- RISC: +77% 2002 to present

Moore’s Law: 2X transistors / “year”

- “Cramming More Components onto Integrated Circuits” Gordon Moore, Electronics, 1965
  - # on transistors / cost-effective integrated circuit double every N months (12 ≤ N ≤ 24)

- Crossroads: Uniprocessor Performance

- Intel 4004 (1971): 4-bit processor, 2312 transistors, 0.4 MHz, 10 micron PMOS, 11 mm² chip
  - RISC II (1983): 32-bit, 5 stage pipeline, 40,760 transistors, 3 MHz, 3 micron NMOS, 60 mm² chip
  - 125 mm² chip, 0.065 micron CMOS = 2312 RISC x86 + FPU + Hauzer + Duache
    - RISC 3 strohs to ~ 6.82 mm² at 65 nm
    - Caches via DRAM or 1 transistor SRAM (www.t-ram.com)?
    - Proximity Communication via capacitive coupling at > 1 TB/s
    (Ivan Sutherland @ Sun / Berkeley)

- Processor is the new transistor?
Problems with Sea Change

- Algorithms, Programming Languages, Compilers, Operating Systems, Architectures, Libraries, ... not ready to supply Thread Level Parallelism or Data Level Parallelism for 1000 CPUs / chip,
- Architectures not ready for 1000 CPUs / chip

Tracking Technology Performance Trends

- Drill down into 4 technologies:
  - Disks
  - Memory
  - Network
  - Processors
- ~1980 Archaic (Nostalgic) vs. ~2000 Modern (Newfangled)

Disks: Archaic (Nostalgic) v. Modern (Newfangled)

- CDC Wren I, 1983
- 3600 RPM
- 0.03 GBytes capacity
- Tracks/Inch: 800
- Bits/Inch: 9550
- Three 5.25" platters
  - Bandwidth: 0.6 MBytes/sec
  - Latency: 48.3 ms
  - Cache: none

Memory: Archaic (Nostalgic) v. Modern (Newfangled)

- 1980 DRAM
  - (asynchronous)
  - 0.06 Mbits/chip
  - 64,000 xtors, 35 mm²
  - 16-bit data bus per module, 16 pins/chip
  - 13 Mbytes/sec
  - Latency: 225 ns
  - (no block transfer)

- 2000 Double Data Rate Synchro.
  - (clocked) DRAM
  - 256.00 Mbits/chip (4000X)
  - 256,000,000 xtors, 204 mm²
  - 64-bit data bus per DIMM, 66 pins/chip (4X)
  - 1600 Mbytes/sec (120X)
  - Latency: 52 ms (4X)
  - Block transfers (page mode)

Latency Lag Bandwidth (for last ~20 years)

- Performance Milestones
  - Disks: 3600, 5400, 7200, 10000, 15000 RPM
  - Latency: 48.3 ms
  - Cache: none

Latency Lag Bandwidth (last ~20 years)

- Performance Milestones
  - Memory Module: 16bit plain
  - DRAM, Page Mode DRAM, 32b, 64b, SDRAM, DDR SDRAM
  - Disk: 3600, 5400, 7200, 10000, 15000 RPM
  - Latency: 52 ms
  - Cache: none
LANs: Archaic (Nostalgic) v. Modern (Newfangled)
- Ethernet 802.3
- Year of Standard: 1978
- 10 Mbits/s link speed
- Latency: 3000 µsec
- Coaxial cable
- Plastic covering
- Braided outer conductor
- Copper core

- Ethernet 802.3ae
- Year of Standard: 2003
- 10,000 Mbits/s link speed
- Latency: 190 µsec (15X)
- Switched media
- Category 5 copper wire

Coaxial Cable: Twist separation: 0.864 in (21.9 mm)
Category 5: 0.7 in (17.7 mm)

*Cat 5* is 4 twisted pairs in bundle
Category 5 copper wire
Latency: 190
link speed
10,000 Mbits/s

Rule of Thumb for Latency Lagging BW
- In the time that bandwidth doubles, latency improves by no more than a factor of 1.2 to 1.4
  (and capacity improves faster than bandwidth)
- Stated alternatively:
  Bandwidth improves by more than the square of the improvement in Latency

CPUs: Archaic (Nostalgic) v. Modern (Newfangled)
- 1982 Intel 80286
  - 12.5 MHz
  - 2 MIPS (peak)
  - Latency 320 ns
- 1998 Intel Pentium 4
  - 500 MHz (120X)
  - 4500 MIPS (peak) (2250X)
  - Latency 5 ns (20X)
- 2001 Intel Pentium 4
  - 134,000 x tors, 47 mm²
  - 64-bit data bus, 423 pins
- 2001 AMD Athlon
  - 3-way superscalar, Dynamic translate to RISC, Superpipelined (22 stage), Out-of-Order execution
- 2001 IBM PowerPC 750
  - 5M x tors, 104 mm²
  - 64-bit data bus, 423 pins
- 2001 Intel Pentium 4
  - 64-bit data bus, 423 pins
- 2001 Intel Pentium 4
  - 3-way superscalar, Dynamic translate to RISC, Superpipelined (22 stage), Out-of-Order execution
- 2001 IBM PowerPC 750
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- 2001 Intel Pentium 4
  - 64-bit data bus, 423 pins

6 Reasons Latency Lags Bandwidth
1. Moore’s Law helps BW more than latency
2. Distance limits latency
3. Bandwidth easier to sell (‘bigger=better’)
4. Latency helps BW, but not vice versa
5. Bandwidth hurts latency
6. Operating System overhead hurts Latency more than Bandwidth
Summary of Technology Trends

- For disk, LAN, memory, and microprocessor, bandwidth improves by square of latency improvement
  - In the time that bandwidth doubles, latency improves by no more than 1.2X to 1.4X
- Lag probably even larger in real systems, as bandwidth gains multiplied by replicated components
  - Multiple processors in a cluster or even in a chip
  - Multiple disks in a disk array
  - Multiple memory modules in a large memory
  - Simultaneous communication in switched LAN
- HW and SW developers should innovate assuming Latency Lags Bandwidth