Memories in General

- Computers have mostly RAM
- ROM (or equivalent) needed to boot
- ROM is in same class as Programmable Logic Devices (PLDs), in which are also FPGAs
  - Lots of memories in these devices
Properties of Memory

• **Volatile**
  ♦ Memory disappears if power goes out
    • Typical computer RAM
    • Palm

• **Nonvolatile**
  ♦ ROM
  ♦ Flash memories
  ♦ Magnetic memories like disk, tape
Random Access Memories

• So called because it takes same amount of time to address any particular part
  ♦ This is not quite true for modern DRAMs
Simple View of RAM

- Of some word size $n$
- Some capacity $2^k$
- $k$ bits of address line
- Maybe have read line
- Have a write line
1K x 16 memory

• Variety of sizes
  ♦ From 1-bit wide

• Memory size specified in bytes
  ♦ This would be 2KB memory

• 10 address lines and 16 data lines
Writing

• Sequence of steps
  ♦ Setup address lines
  ♦ Setup data lines
  ♦ Activate write line
Reading

• Steps
  ♦ Setup address lines
  ♦ Activate read line
  ♦ Data available *after specified amt of time*
Chip Select

• Usually a line to *enable* the chip
• Why?

<table>
<thead>
<tr>
<th>Chip select CS</th>
<th>Read/Write R/W</th>
<th>Memory operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>×</td>
<td>None</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Write to selected word</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Read from selected word</td>
</tr>
</tbody>
</table>
Static vs Dynamic RAM

- **SRAM vs DRAM**
- **DRAM stores charge in capacitor**
  - Disappears over short period of time
  - Must be refreshed
- **SRAM easier to use**
  - Faster
  - More expensive per bit
  - Smaller sizes
Structure of SRAM

- Control logic
- One memory *cell* per bit
  - Cell consists of one or more transistors
  - Not really a latch made of logic
- Logic equivalent
Bit Slice

- Cells connected to form 1 bit position
- Word Select gates one latch from address lines
- Note it selects Reads also
- B (and B not) set by R/W, Data In and BitSelect
Bit Slice can Become Module

• Basically bit slice is a X1 memory

• Next
16 X 1 RAM
Row/Column

- If RAM gets large, there is a large decoder
- Also run into chip layout issues
- Larger memories usually “2D” in a matrix layout
16 X 1 as 4 X 4 Array

- Two decoders
  - Row
  - Column
- Address just broken up
- Not visible from outside
Realistic Sizes

• Imagine 256K memory as 32K X 8
• One column layout would need 15-bit decoder with 32K outputs!
• Can make a square layout with 9-bit row and 6-bit column decoders
SRAM Performance

- Current ones have cycle times in low nanoseconds (say 2.5ns)
- Used as cache (typically onchip or offchip secondary cache)
- Sizes up to 8Mbit or so for fast chips